SPECIFICATION AMENDMENTS

Please amend the paragraph beginning on page 4, line 30, as follows:

Turning now to the figures, wherein like reference numerals represent like elements in all of the several views, Fig. 1 illustrates a network architecture for a telecommunication system 2 that provides VTOA support in accordance with the invention. The system 2 includes plural Packet Voice Gateways (PVG)s 4 that provide bearer and data traffic interconnections between an ATM core network 6 and circuit switched networks 8. The circuit switched networks 8 comprise conventional circuit switched network switching entities 10~~12~~, which are shown as being End Offices (EO)s that would each typically support a base of local loop subscribers (not shown) and other telephone/data customers, such as PBX, dial-up modem and fax.

Please amend the paragraph beginning on page 10, line 28, as follows:

For example, to set up a TDM/ATM interworking AAL1 channel, a PCC~~PPC~~ application calls a corresponding set of API functions while specifying a TDM channel number and an ATM VPI/VCI pair respectively determined from the pools of free TDM CICs and free ATM VCs available at the circuit emulation board 40. Note that the VPI/VCI~~vpi/vci~~ mappings on AAL1 Tx (Transmit) and Rx (Receive) can be independent. However, it is more practical to use the same ATM channel for both directions of routing through the ATM network. If the device driver returns with a "success" return value, the channel is up and ready for use.

Please amend the paragraph beginning on page 11, line 5, as follows:

For a AAL3/4/5 data channel, the device driver API functions are different from the ones used for AAL1 traffic. For example, a PCC application may request that an ATM channel with vpi/vci of 789/9876 to be mapped to an AAL5 VCCI (Virtual Channel Connection Identifier) of 15. This VCCI could be a data link layer channel allocated by a transport upper layer. Typical

examples are TCP/IP for classical IP over ATM (RFC1483/1577), UNI signaling for B-ISDN and SS7 signaling over High-speed link for N-ISDN. Again, if the device driver returns with a "success" return value, the channel is up and ready for use.

Please amend the paragraph beginning on page 11, line 18, as follows:

After a channel request is received from a PCC application, the device driver in the board controller 46 coordinates the ATM cell handling devices of the circuit emulation board 40, namely, the CAM 50, the MUX1 52, the SAR 54 (if necessary), the OAM 56, MUX2 58 and the SARs 60, to set up the required path with a suitable QoS. To that end, and as described in more detail below, the device driver is programmed to establish a header translation scheme which guarantees that ATM cells received at the circuit emulation board 40 are routed to the correct ATM cell handling devices. An internal routing table (described in more detail below with reference to Fig. 4) is constructed based on the routing capabilities of the individual ATM devices.

Please amend the paragraph beginning on page 12, line 7, as follows:

It will be appreciated that different routing tables may be used for different circuit emulation boards, depending on the set of ATM cell handling devices that are present on each board. However, the basic routing concept remains the same for all boards. The goal is to "compact or condense" a large 28-bit VPI/VCI ~~vpi/vci~~ address space into a 2048 TDM on-board address space.

Please amend the paragraph beginning on page 13, line 3, as follows:

In step 76, the AAL1 cell stream generated by the traffic handling SAR 60 is multiplexed by the MUX2 58 in its 8-to-1 mode. In step 78, the ATM cells are sent to the OAM 56. A check for locally generated OAM cells is made in step 80 and, if found, such cell are interleaved into

the cell stream in step 81. In step 82, the ATM cells are then sent to MUX1 52 and then on to the ATM framer/deframer 48 in step 84 for framing and transmission by the optical transceiver 44.

Please amend the paragraph beginning on page 14, line 4, as follows:

Persons skilled in the art will appreciate that a CAM permits the rapid lookup of stored data using the data itself to find a storage address, rather than a storage address to find the data. CAM/RAM combinations have been used successfully in ATM switches to rapidly rewrite new VPI/VCI~~VPI/VPI~~ cell header information to ATM cells as they are passed from one VC link segment to another along a VCC. In particular, when an incoming cell arrives at an ATM switch, a CAM lookup is performed using the cell header VPI/VCI information. When a match occurs, the address associated with the provisioned VPI/VCI information is used to access a RAM containing the VPI/VCI cell header information for the next hop. This new information is written to the cell header and the cell is sent along to the next ATM switch.

Please amend the paragraph beginning on page 14, line 23, as follows:

Although various translation schemes may be used to implement the invention, the circuit emulation board 40 implements a four-element cell header mapping strategy in which four bit fields of the untranslated cell header "H1" are rewritten with routing information for use by the downstream cell handling components of the circuit emulation board. In particular, and with additional reference now to Fig. 4, a first bit field "A," representing Generic Flow Control (GFC) bits 3 and 2 of the untranslated cell header H1, is rewritten with values of either "0" or "1." This information is used by MUX1 52 to route AAL5 cells to the signaling SAR 54 (if GFC bit 2 contains a "1"~~"0"~~) and to route AAL1 cells to the OAM 56 (if GFC bit 2 contains a ~~"0"~~"1"). Note that GFC bit 3 is not actually used by the circuit emulation board 40 in the illustrated embodiment in which MUX1 52 acts as a 1:2 demultiplexer for separating AAL1 and AAL5

traffic. However, by using GFC bit 3, 1:4 demultiplexing could be implemented such that additional adaptation layer cell types, such as AAL0 and AAL 3/4 could be processed.

Please amend the paragraph beginning on page 15, line 10, as follows:

A third bit field "C," representing VPI bits 2-0 of the untranslated cell header H1, is rewritten with values of either "0" or "1." This information, which can provide eight different values, is used by MUX2 58 as a traffic handling SAR identifier as it performs 1:8 demultiplexing. It will be seen that the "C" column for VPI bits 2-0 in the table of Fig. 4 has some entries that read "any" and other entries that read "=user." The "any" entry designates a translated value and the "=user" entry designates a translated F5 VPI/VCI~~vpi/vci~~ that is carried over from the corresponding translated "any" value on a user channel. In the table of Fig. 4, the "any" entry for AAL1 cells appears in the "C" column. The "any" value can be conveniently assigned in a round robin or circular fashion initially so that sequential PCC requests are evenly distributed among different ports of the SARs 60. But as calls are set up and torn down randomly, the "any" values will end up being assigned from a free pool of size 2048. It should be noted that other columns of the table of Fig. 4 have a third entry that reads "x." The "x" entry is a "don't care" designation because these header values will not be examined (i.e., they will be ignored) by the various ATM devices chosen for the circuit emulation board 40 and hence can be set to 0 in the CAM look-up table 50a. Note that the CAM look-up table size is determined by the total number of supported channels for the various AAL types handled by the circuit emulation board 40.